13.6 A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13µm CMOS

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High-performance wired communication systems call for high-resolution medium-bandwidth ADCs. Wideband interferers are present in many environments. Sufficient anti-alias filtering is necessary in order to prevent in-band SNR degradation, but high-order high-Q filters are often not efficient in terms of area and power consumption. To relax the filter requirements even traditional Nyquist-rate converters such as pipeline and SAR ADCs are operated with OSR>1. In [1], a very effective concept of a SAR ADC with redundancy was introduced. It is the objective of this work to introduce techniques to increase the sample rate, clock frequency, and linearity of the SAR ADC beyond its present-day limitations. The block diagram of such an ADC is shown in Fig. 13.6.1. Only the anti-aliasing filter(AAF) requires a highly linear opamp. A large fraction of the ADC is digital circuitry, which makes this concept attractive for implementation in present and future deep submicron technologies with low supply voltages. The row and column decoders translate the binary output of the logic block to thermometer code and address the local decoders inside the capacitor array as suggested in [1]. The reference buffer stabilizes the bottom plate voltage of the capacitors inside the array. The top plates of all cells are connected to a common rail, allowing charge to redistribute after a change of the digital input of the array. The PLL merely generates the iteration clock while the input voltage is sampled directly by the high-quality clock. Therefore, a power and area efficient ring oscillator PLL can be used without degrading the ADC performance. This converter provides an opportunity of by-2 interleaving without much additional effort, thus doubling the sample frequency. One ADC iterates while the other samples the AAF output. All blocks except C-array and comparator are common to both sub converters.

Figure 13.6.2 shows the simplified functional diagram of a SAR ADC. The non-binary step sizes for each iteration with redundancy are stored in the ROM. Two adders calculate the sum S=Y+R and the difference D=Y-R of the ROM output and the previous effective binary value on the bus in parallel. The results are stored in 2 registers. Depending on the current state of the comparator output, the multiplexer sends the pre-calculated result, Y, onto the bus towards the decoder. The latter converts the binary data from the processing unit to thermometer-coded vectors, necessary to control the row and column lines of the unity capacitor array. In the circuit realization, the 3 functions S/H, DAC, and building the sum of both, the residual voltage v_R, are concentrated in the array. The residual voltage is amplified and then applied to the comparator, which in turn controls the multiplexer. In Fig. 13.6.2, for each functional block in the time-critical decision path, the associated delays t1 through t4 are depicted. The timing values in the table are worst-case delays, simulated in 0.13µm CMOS, including wiring capacitance.

For the following considerations, it is assumed that the sampling clock is f_S=40MHz, the number of iteration steps per conversion is 12 and the iteration clock frequency, f_I, equals $12 \cdot f_S$=480MHz. The corresponding period, T, is about 2.1ns. Summing t1 to t4 leaves a settling time of 0.1ns for the preamplifier. SPICE simulations show that the preamp requires a minimum of 0.8ns, since a gain of <40dB does not guarantee accurate decisions during the last iteration steps of each conversion. Jitter of the PLL clock, which will further decrease the settling margin, has not yet been considered. Therefore, it is concluded that under the assumed conditions the structure suggested in [1] and depicted in Fig. 13.6.2 is not feasible. Consequently, a structural change is mandatory, to enable the SAR ADC to be reliably used with the intended clock frequency.

The proposed solution is shown in Fig. 13.6.3. Essentially, the decoder is shifted out of the critical path, reducing its delay by t3=0.7ns to achieve 0.86ns. Thus, the 0.8ns requirement is met. However, now the multiplexer needs to be fed by 2 independent decoders that again expect a sum-difference pair Y_S and Y_D at their inputs (cf. S, D in Fig. 13.6.2). To allow the decoding process to take place in a separate clock cycle, the pre-decoded values are buffered in additional registers. The information on Y_S and Y_D is one clock cycle ahead of that on Y in Fig. 13.6.2. This predictive data is generated by preprocessing 2 sums, S_S and S_D, and 2 differences, D_S and D_D. The set of possible outcomes is now complete.

The method in Fig. 13.6.2 can be considered as a 2-stage pipeline, with the preprocessing of S and D in stage 1, and the decoding, analog functions, and comparison in stage 2. The latter stage is overloaded with delays, resulting in a bottleneck for operating speed. Accordingly, the method in Fig. 13.6.3 is a 3-stage-pipeline, by inserting an additional stage for the decoders, thus resolving the speed problem.

The previous calculations assumed that the preamp would settle within 0.8ns. This was not possible without fundamentally altering the ubiquitous resistively loaded differential pair.

Figure 13.6.4 shows the amplifier used in this ADC. During the sample phase while reset is high, the capacitors store the offset voltages of the respective stages. During the iteration process reset is low and the residual voltage v_R is amplified by the capacitively coupled chain. As long as v_R is reasonably small, not driving the output of any stage to saturation, the chain operates at its small-signal bandwidth. However, during the iteration v_R shows a highly dynamic behavior, decaying exponentially from the order of the reference voltage down to a few-hundred microvolts. As soon as one stage is saturated by a large signal, it saturates the subsequent one. Recovering several consecutive stages from saturation, e.g., when a small v_R follows a large v_R, leads to excessive delay. To eliminate this effect, transistors P1 are switched on at the beginning of each conversion and released stage by stage during the iteration. Thus, both gain and bandwidth of each stage are adapted to the expected signal swing. Incorporating this feature results in a reduction of the maximum preamp delay to the value assumed above.

The chosen OSR allows the use of DEM which is introduced in the form of a barrel-shift algorithm. The frequency spectrum in Fig. 13.6.5 shows the measured performance. Figure 13.6.6 summarizes the key properties of the presented SAR ADC design while Fig. 13.6.7 shows the layout of the test chip.

Acknowledgement:
The authors would like to thank Thi-Nga Do, for her excellent layout work and her patience during the numerous changes throughout the design.

Reference:
[1] F. Kuttner, "A 1.2V 10b 20MSamples/s Non-Binary Successive Approximation ADC in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 176-177, Feb., 2002.

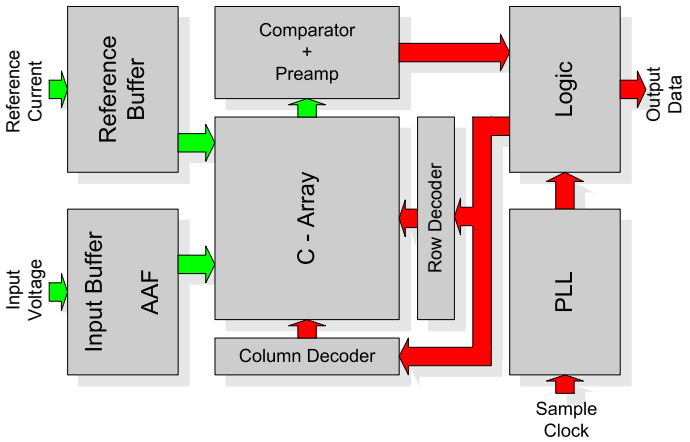

Figure 13.6.1: Block diagram of SARADC.

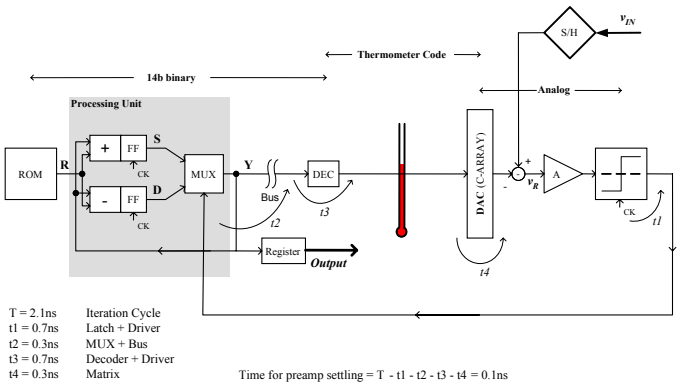

Figure 13.6.2: Two-stage pipeline.

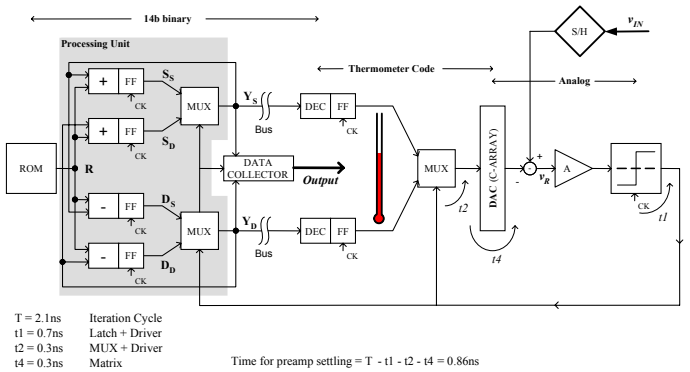

Figure 13.6.3: Three-stage pipeline.

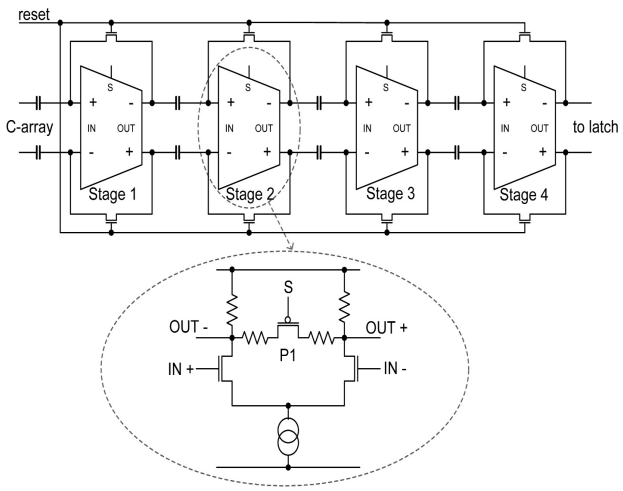

Figure 13.6.4: Pre-amplifier circuit.

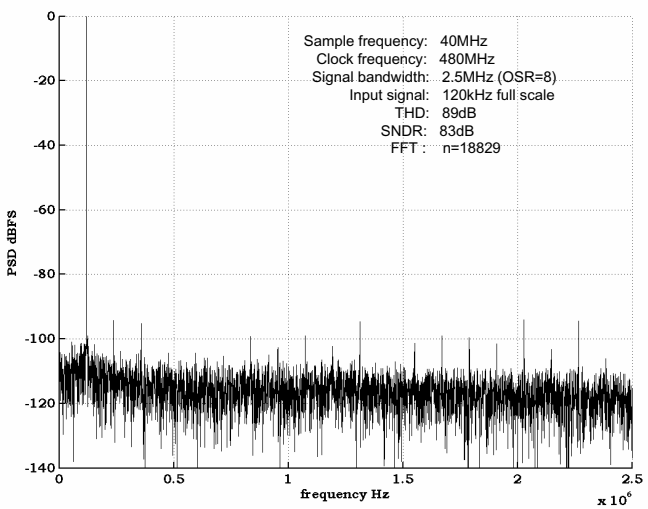

Figure 13.6.5: Measured frequency spectrum of the output.

Power supply voltage	1.5V
Input range	±0.9V differential
Sampling frequency	40MHz
Clock frequency	480MHz
Analog power consumption	49mW
Digital power consumption	17mW
Total power consumption	66mW
Resolution	14b
THD/SNDR at 120kHz FS	89dB/83dB at OSR=8
THD/SNDR at 480kHz FS	87dB/83dB at OSR=8
THD/SNDR at 960kHz FS	87dB/83dB at OSR=8
Noise floor	-85dBFS at OSR=8
Area (ADC, PLL, Ref. buffer, AAF)	0.55mm²
Technology	0.13µm 1P5M CMOS

Figure 13.6.6: Performance summary.

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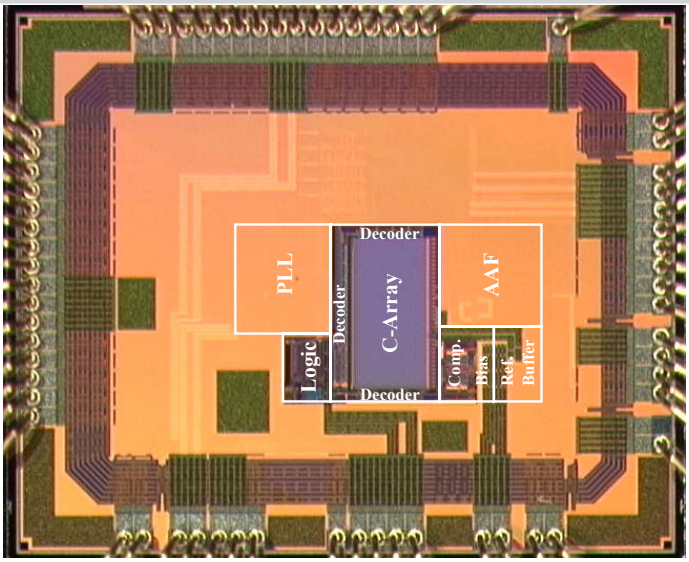

Figure 13.6.7: Test chip micrograph.

